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MS-7392

Version: 2.1

CPU:

Intel Pentium 4, Pentium D, Core2 Duo, Wolfdale, Kentsfield and Yorkfield processors in LGA775 Package.

System Chipset:

Intel - MCH (North Bridge) P31
Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI EEPROM
HD Codec -- ALC888
LPC Super I/O -- F81182
LAN-- REALTEK RTL8111C/8111B
CLOCK -- ICS9LPRS514EGLF

Main Memory:


DDR II * 4 (Max 4GB)

Expansion Slots:

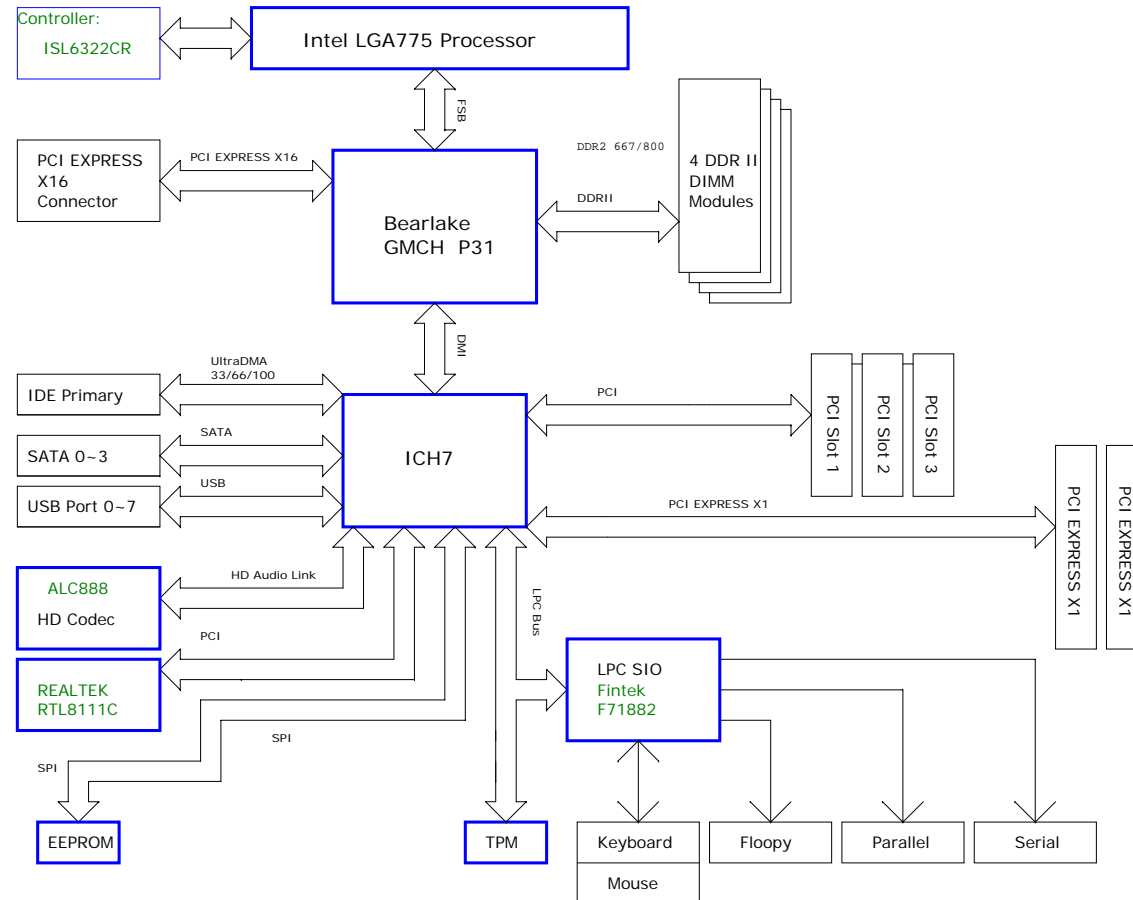
PCI2.3 SLOT * 3
PCI EXPRESS X1 SLOT * 1
PCI EXPRESS X16 SLOT


INTELSIL PWM:

Controller: INTELSIL - ISL6322CR

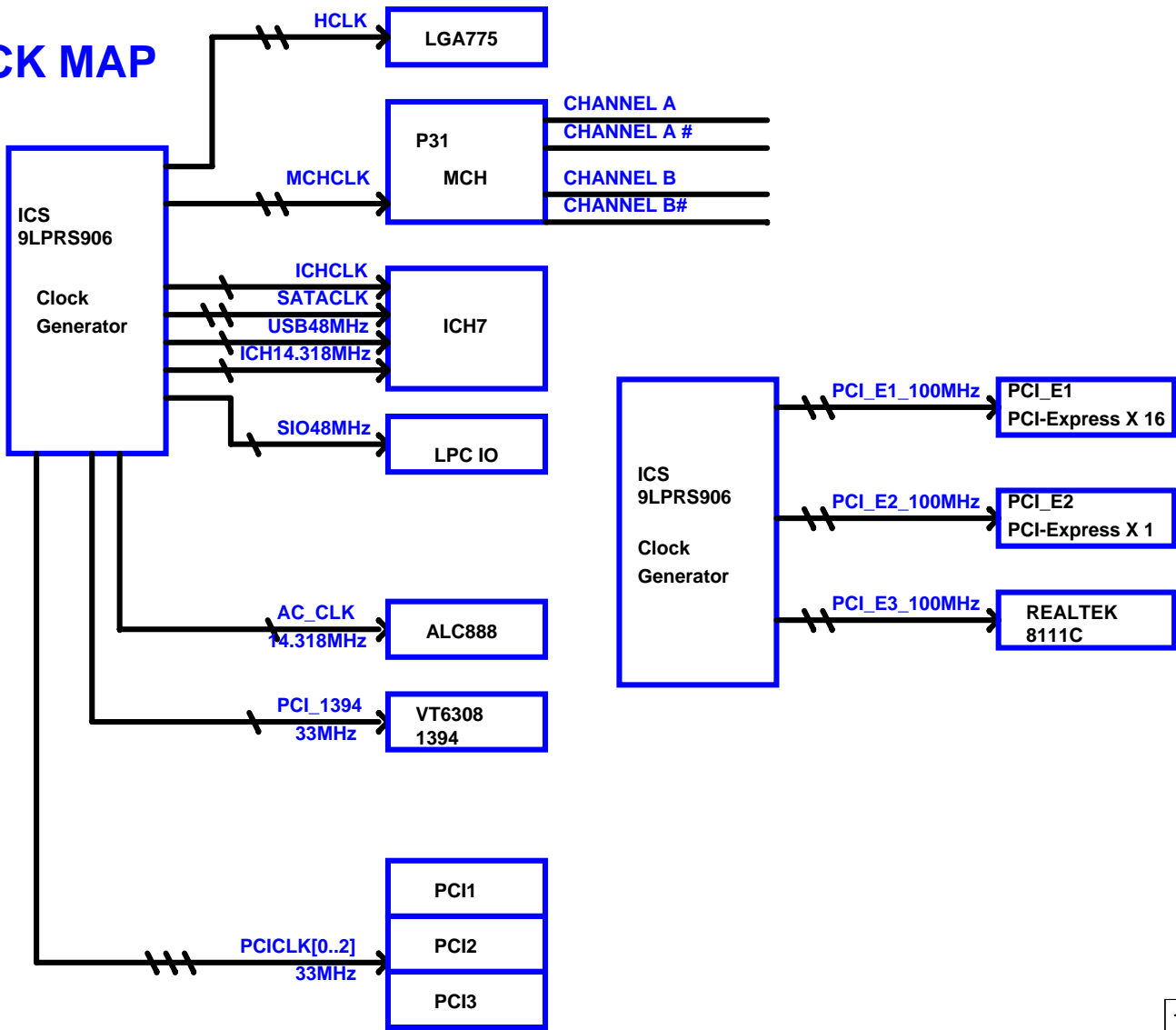
 MICRO-STAR INT'L CO., LTD.		
Title COVER SHEET		
Size	Document Number MS-7392	Rev 2.1
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Block Diagram

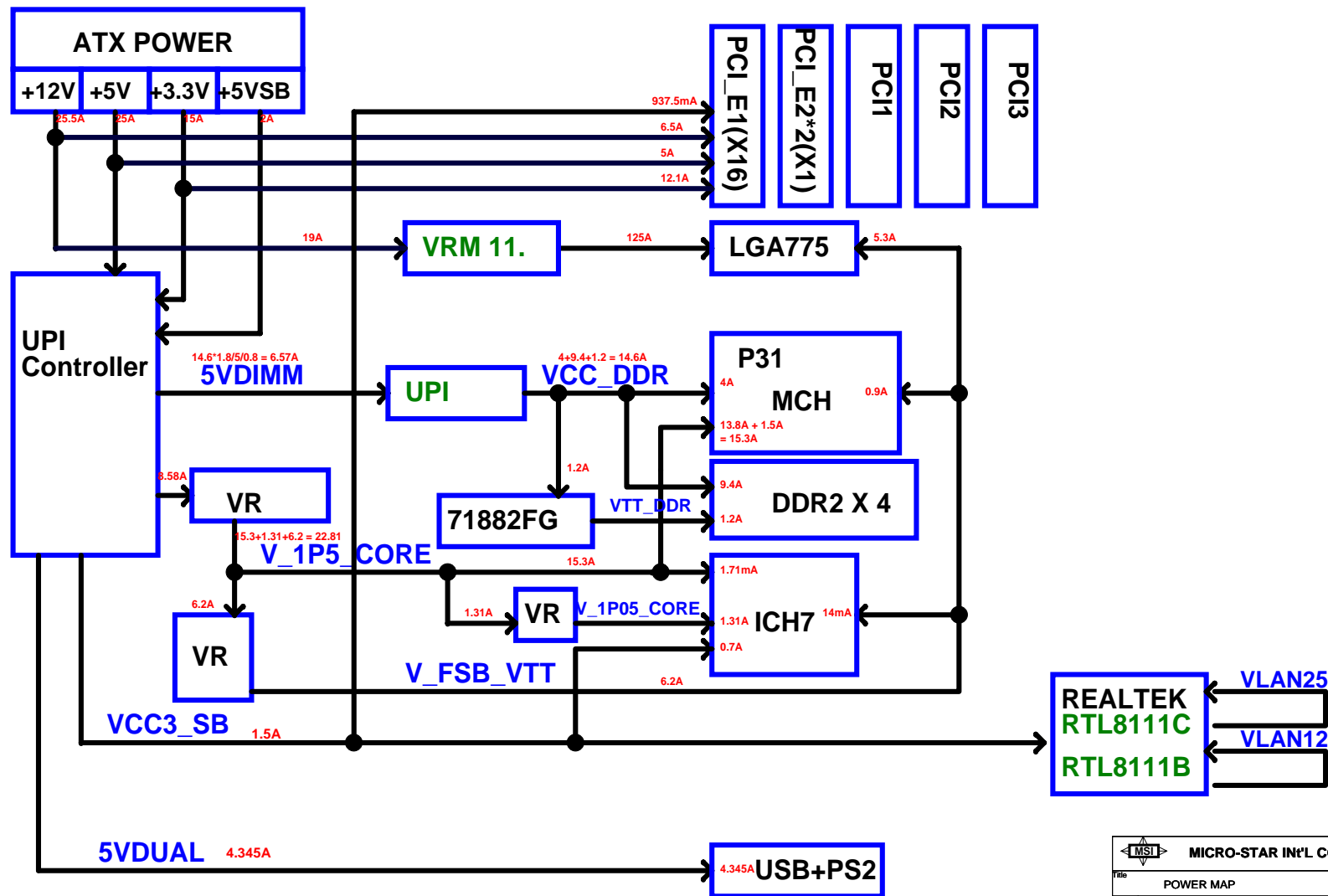


		MICRO-STAR INT'L CO., LTD.	
Title			
BLOCK DIAGRAM			
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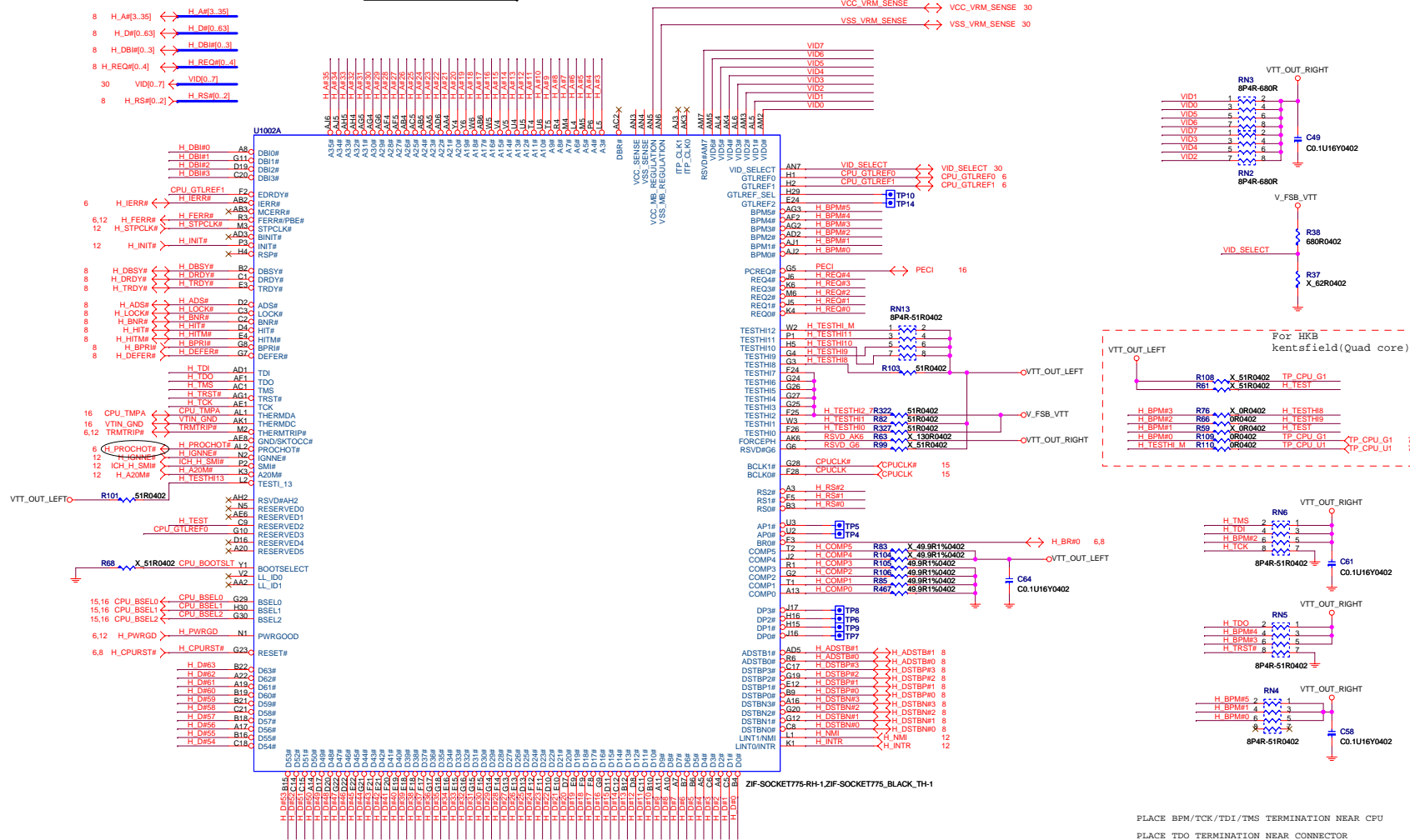
CLOCK MAP



POWER MAP



CPU SIGNAL BLOCK



PLACE BPM/TCK/TDI/TMS TERMINATION NEAR CPU
PLACE TDO TERMINATION NEAR CONNECTOR



MICRO-STAR INT'L CO., LTD.

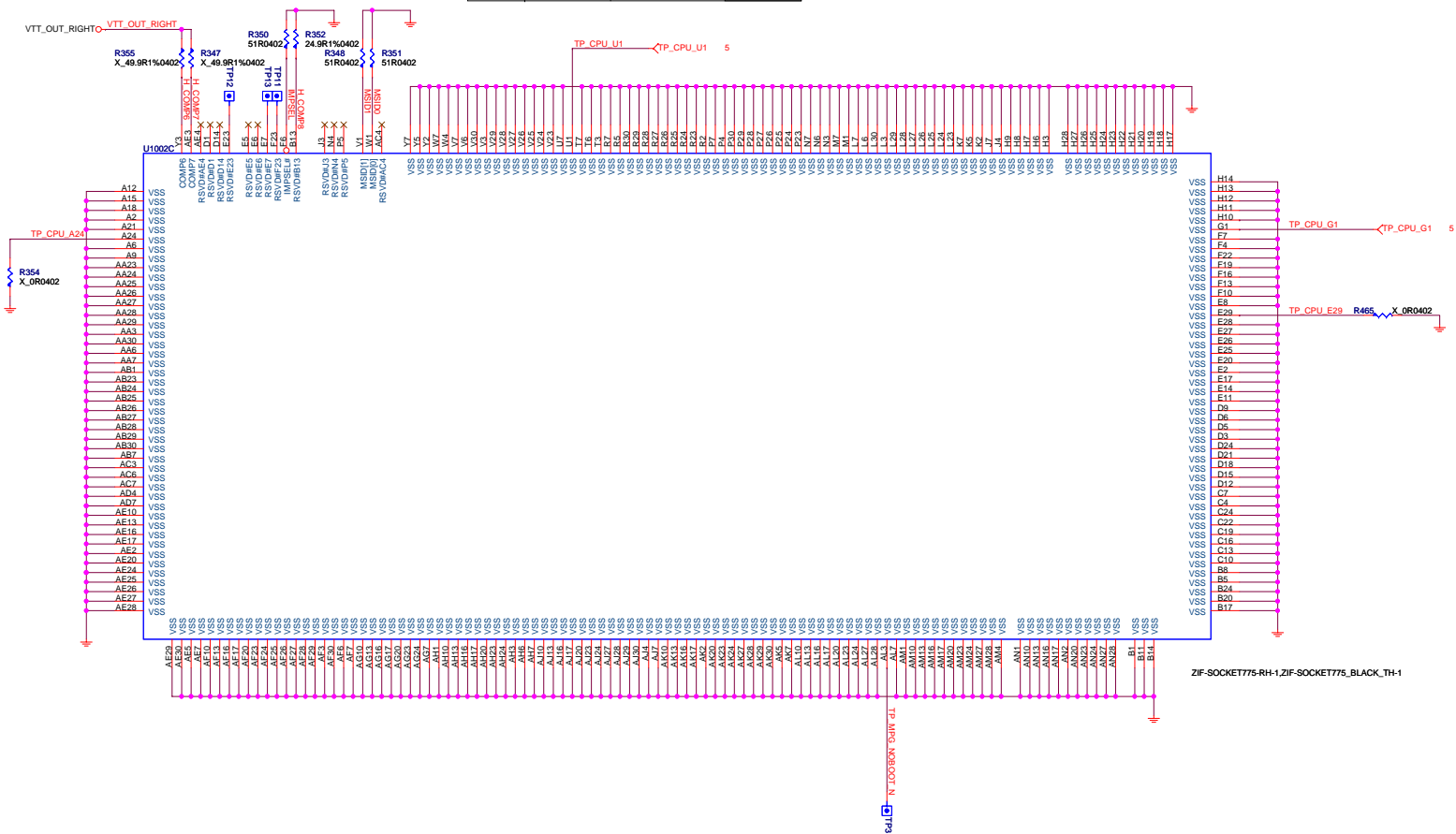
Title	Intel LGA775 CPU - Signals
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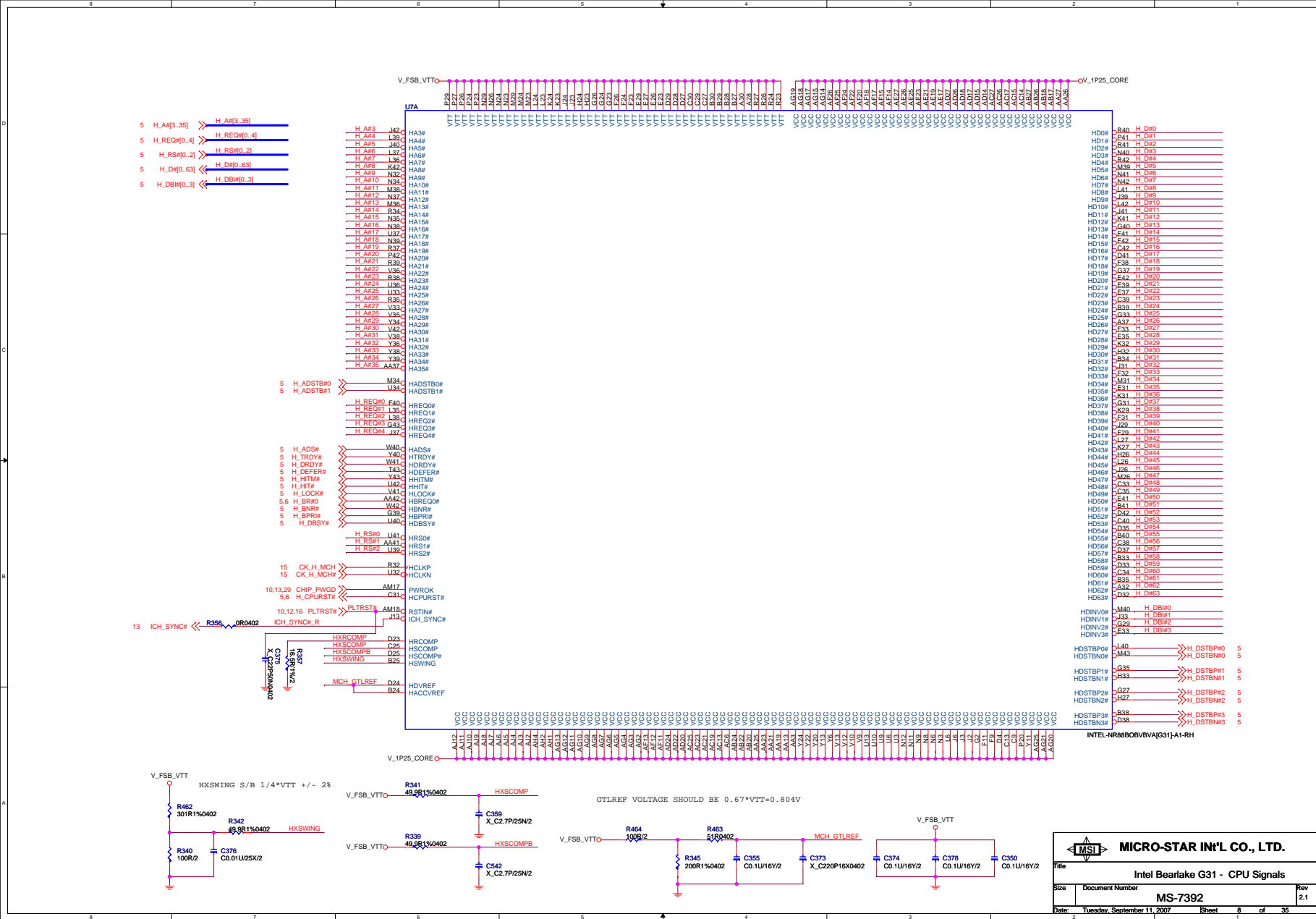
Size	Document Number
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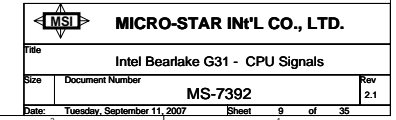
MS-7392

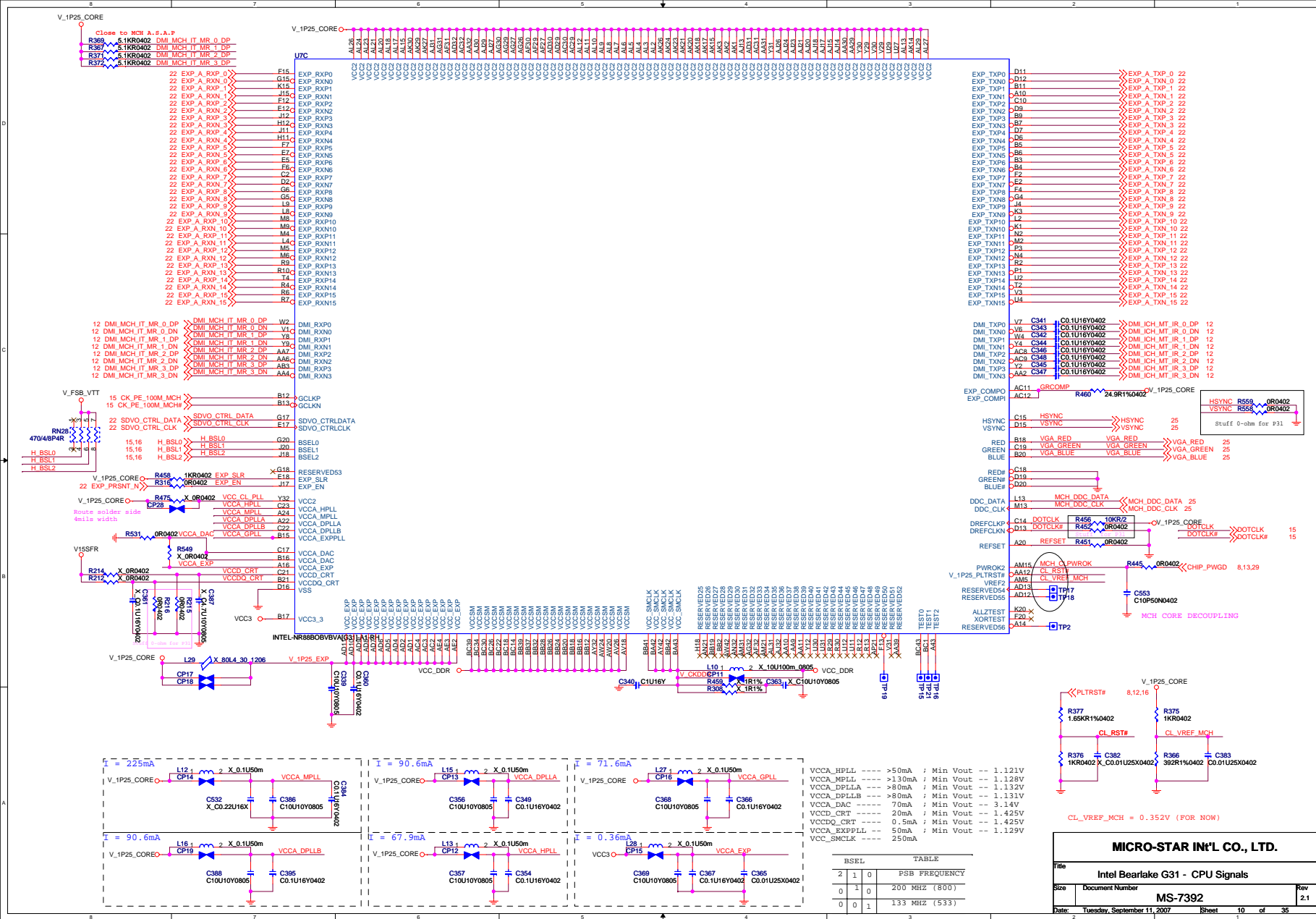
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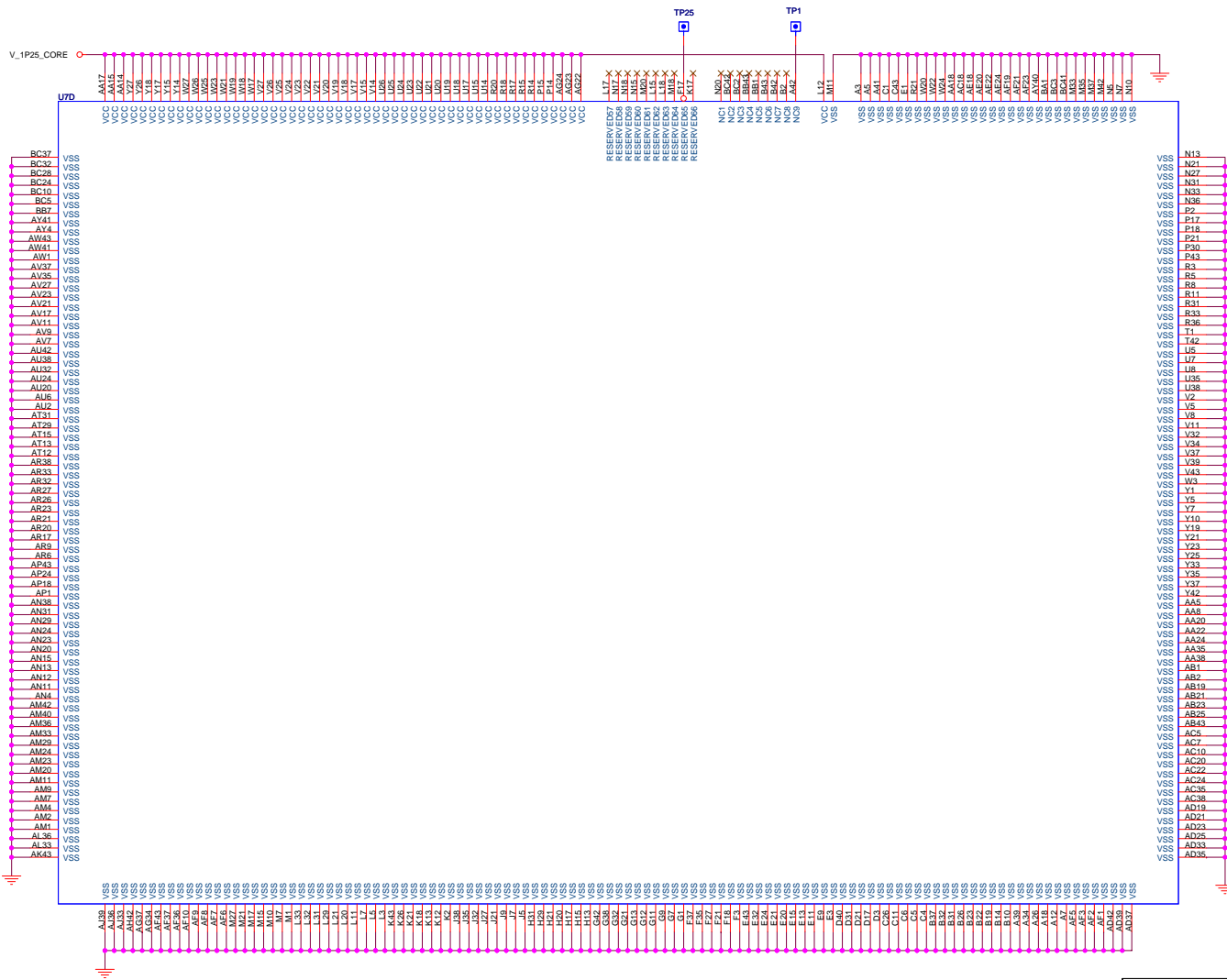
	2005 Performance PMB platform 1	2005 Mainstream/Value PMB platform 2	2006 65W PMB platform 3
MSID1	0	0	0
MSID0	0	NC	NC



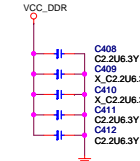




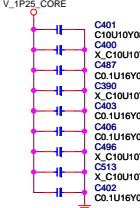




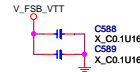
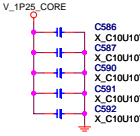
Place close to GMCH




MCH CORE DECOUPLING

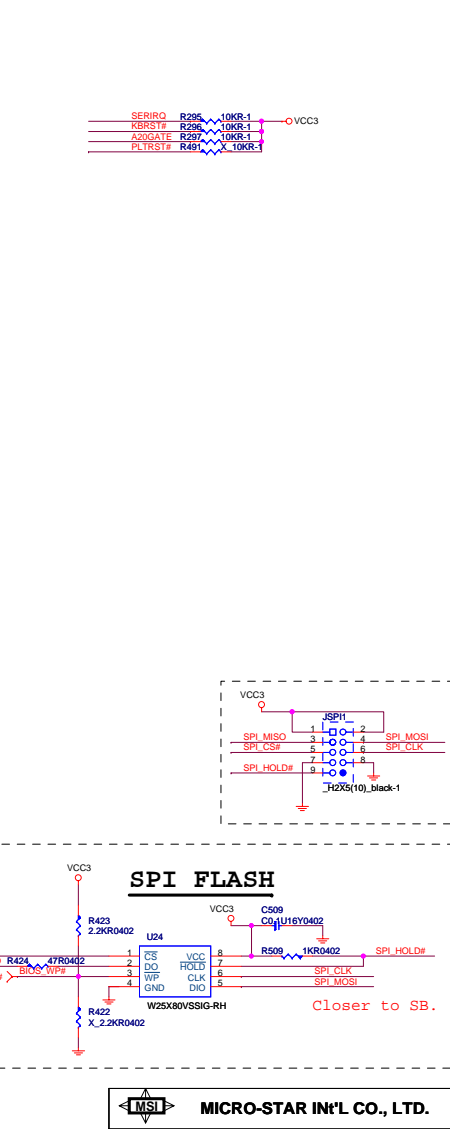
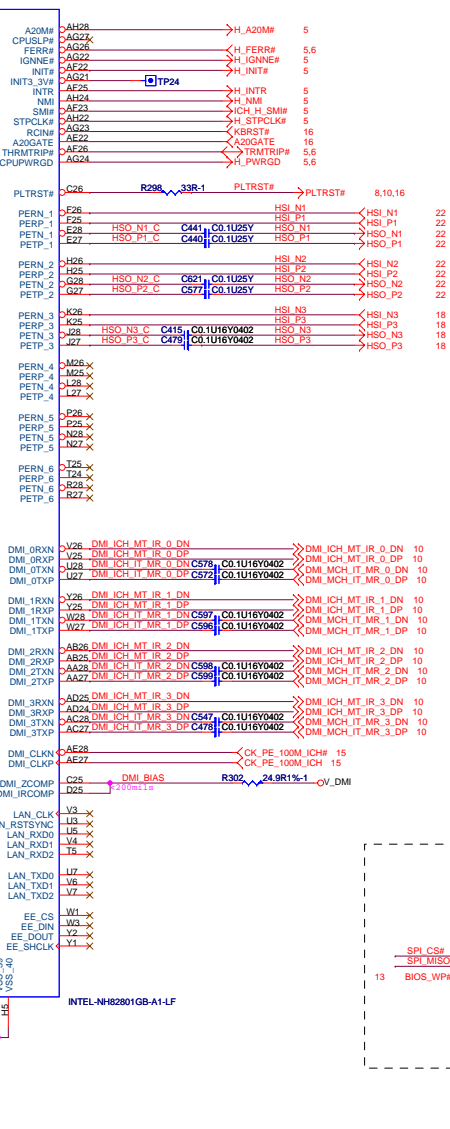
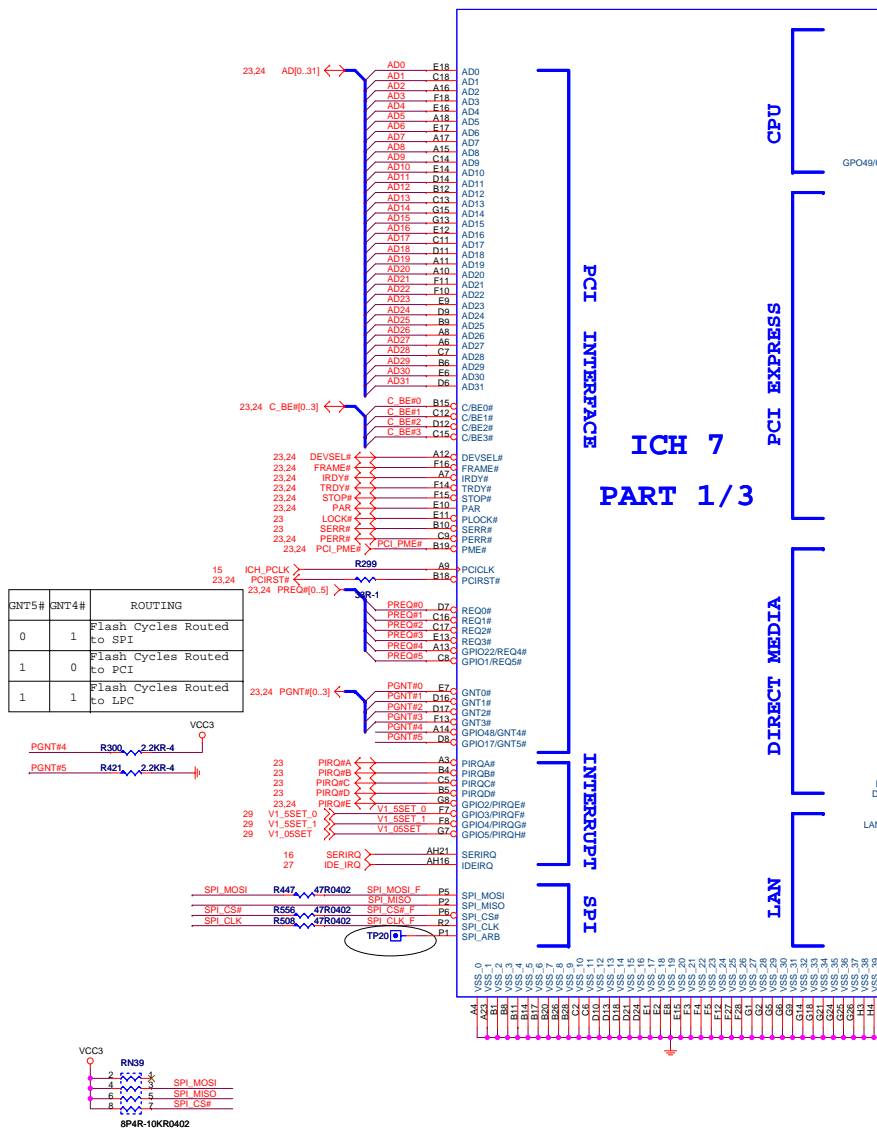


5020 Parts

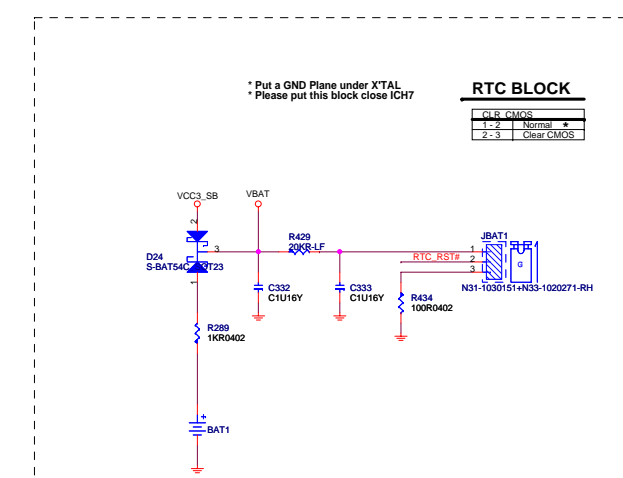



INTEL-NR88B08VBVA/G31J-A1-RH

 MICRO-STAR INT'L CO., LTD.		
Title Intel Bearlake G31 - CPU Signals		
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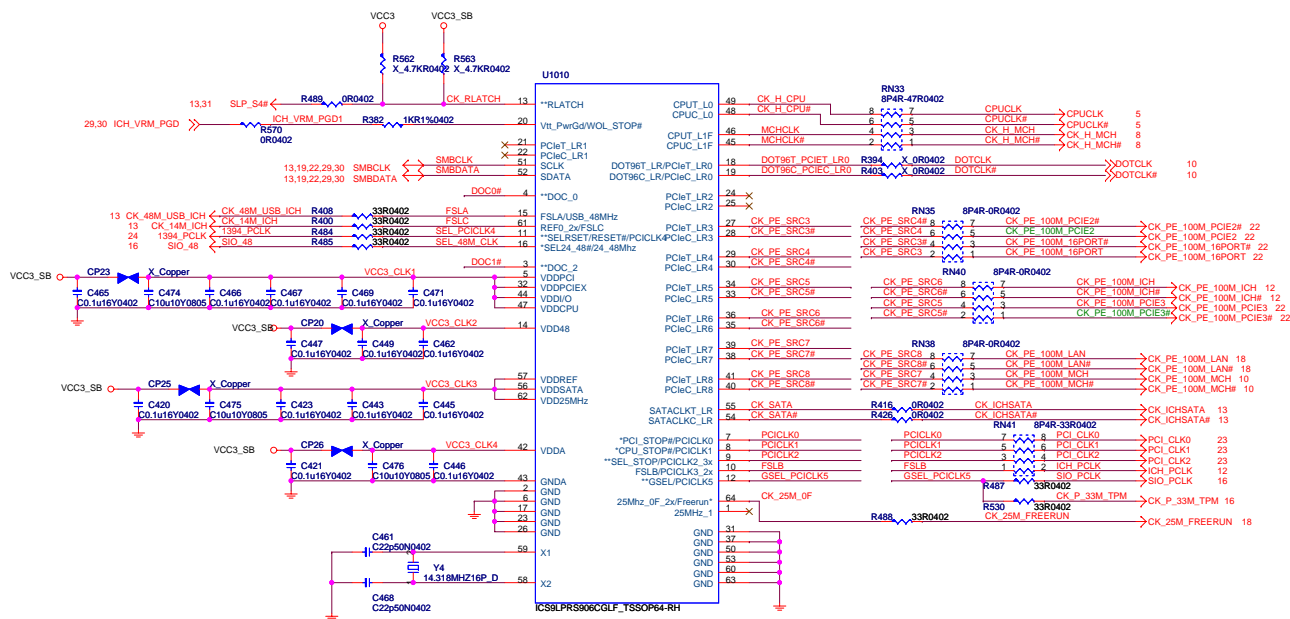


GNT5#

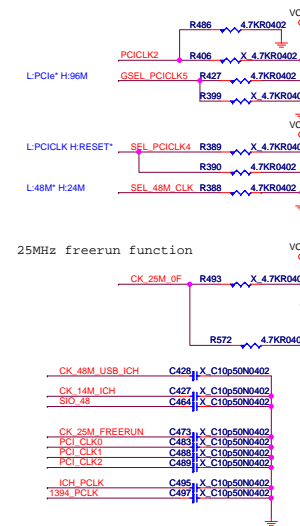


 MICRO-STAR INT'L CO., LTD.	
Title Intel ICH7 - LPC & ATA & USB & GPIO	
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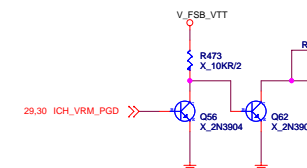
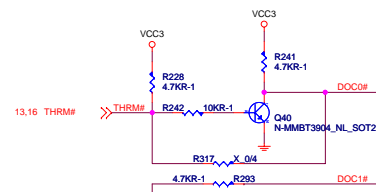
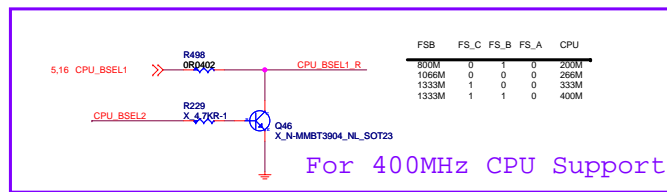
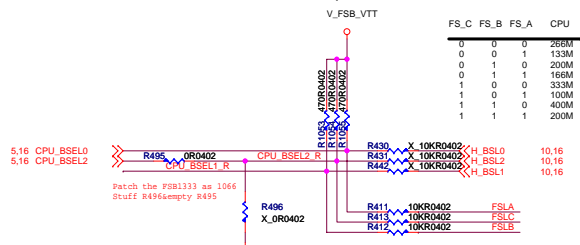
Clock Generator - ICS9LPRS906CGLF



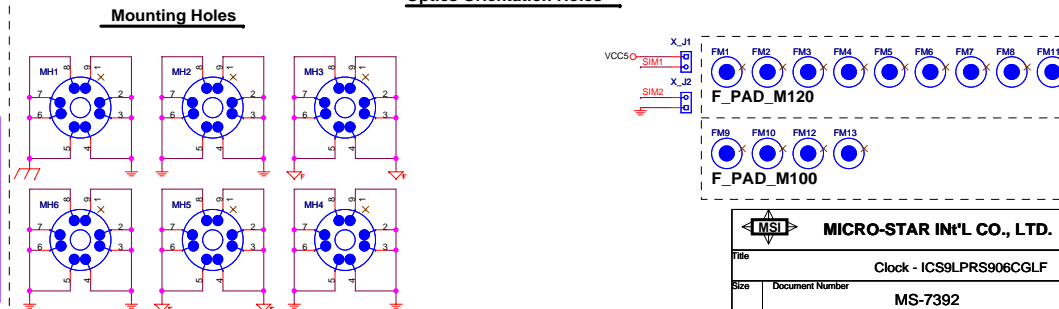
CLOCK GEN STRAPING

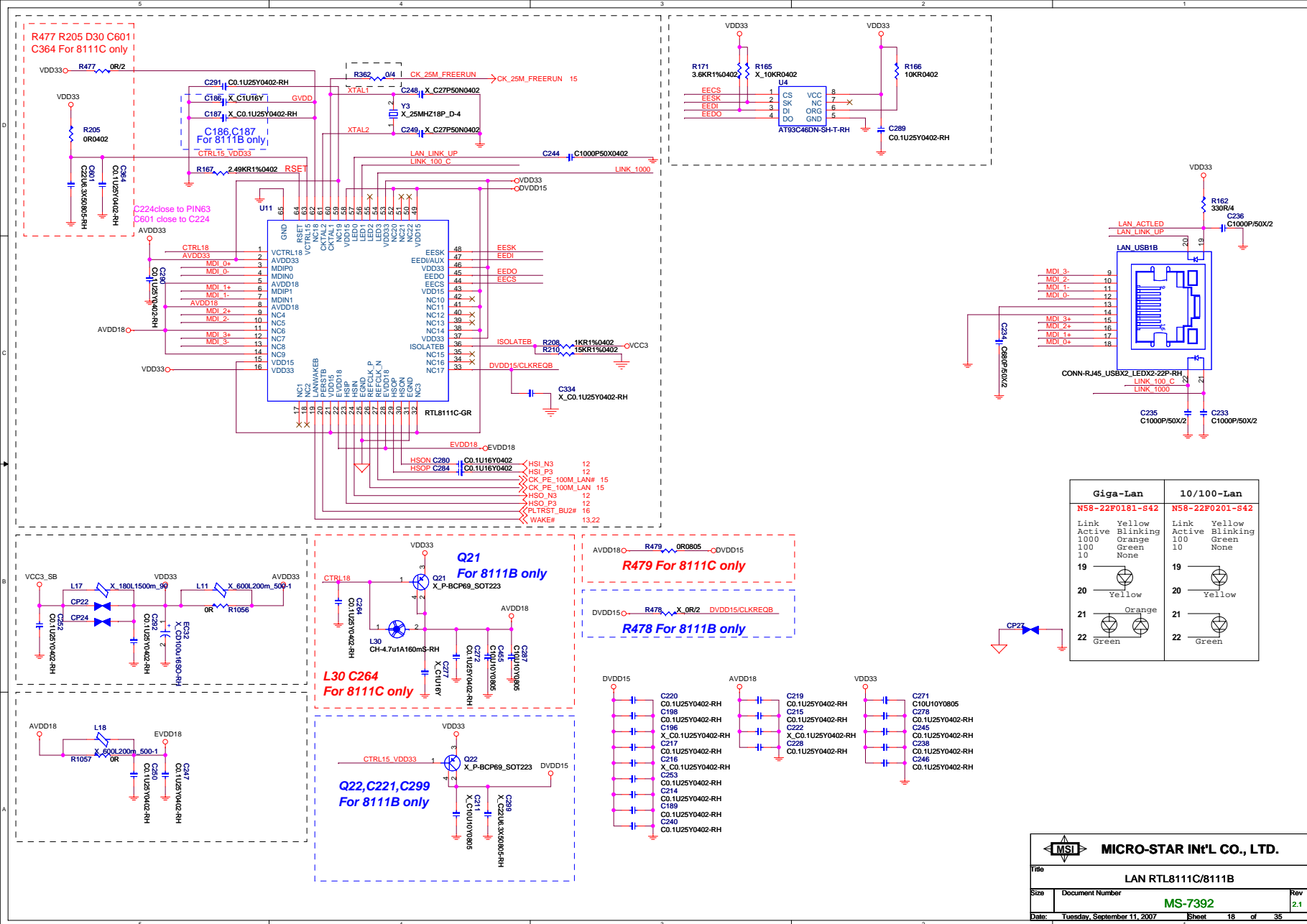





CPU Frequency Selection



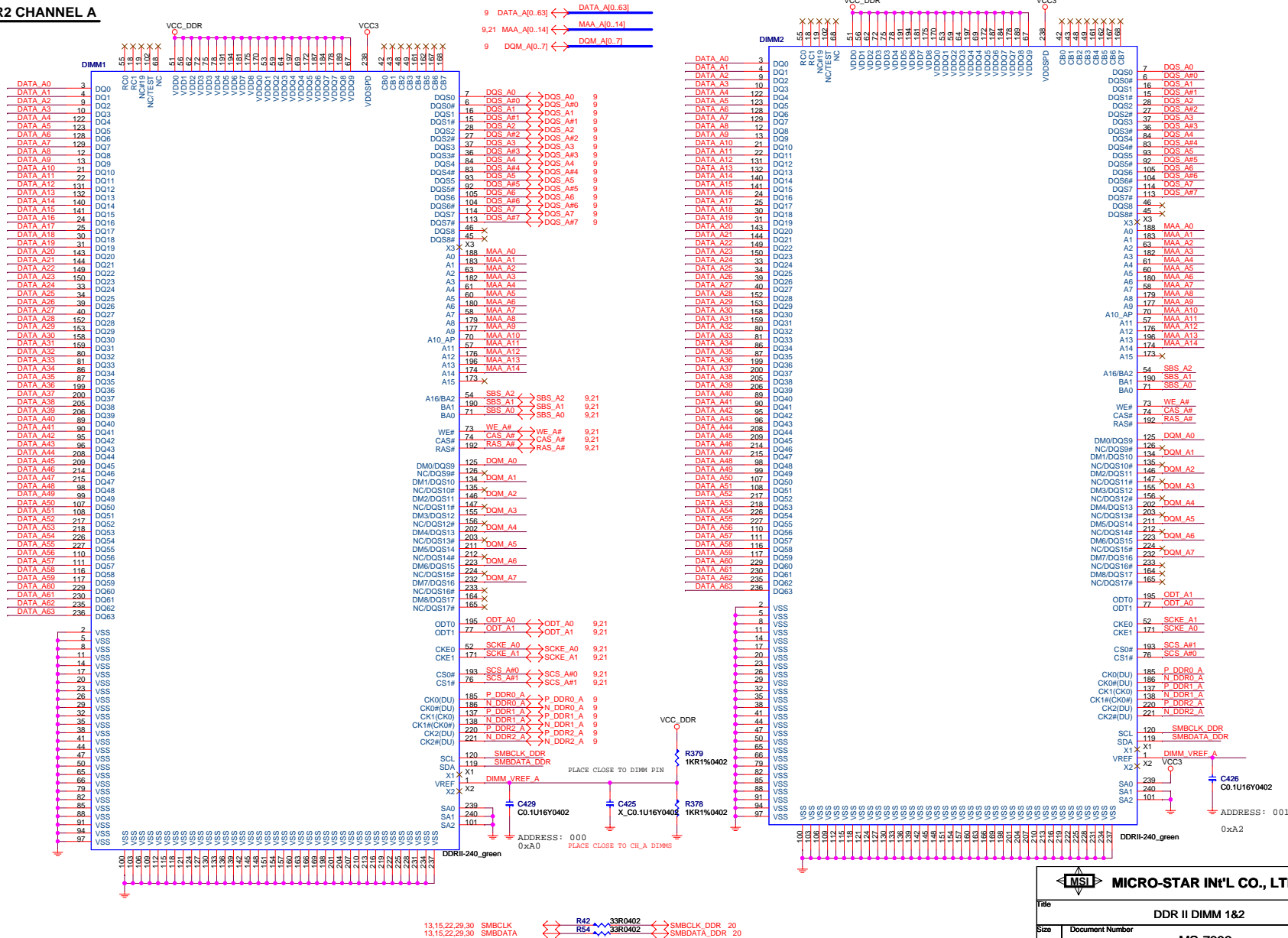
Optics Orientation Holes



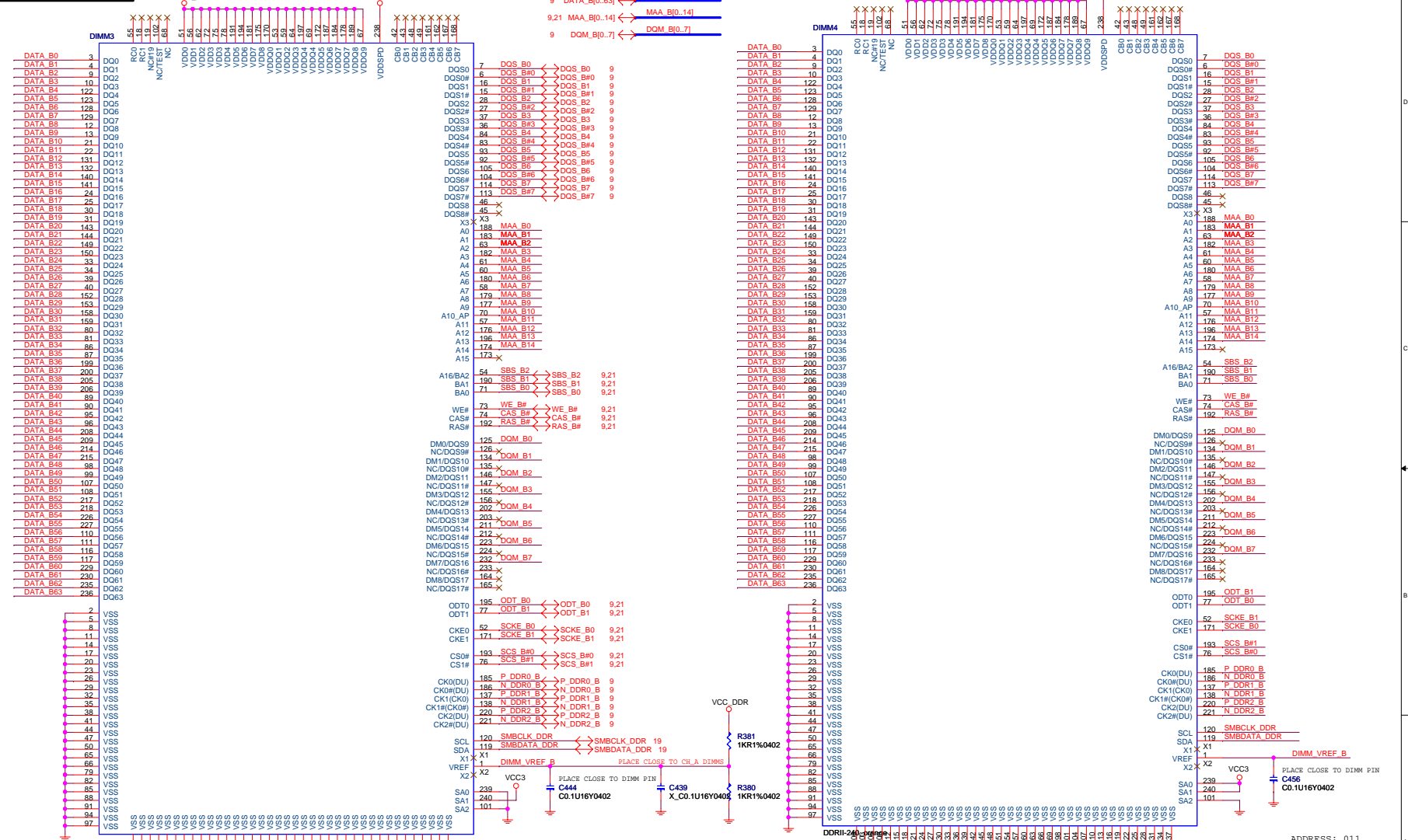



Giga-Lan		10/100-Lan	
N58-22P0181-S42		N58-22P0201-S42	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

DDR2 CHANNEL A



DDR2 CHANNEL B



**MICRO-STAR INT'L CO., LTD.**

Title

DDR II DIMM 3&4

Size

Document Number

MS-7392

Rev

2.1

Date:

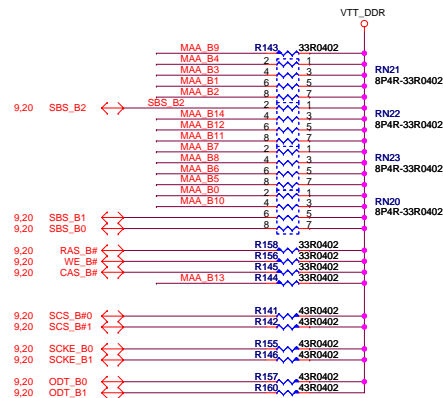
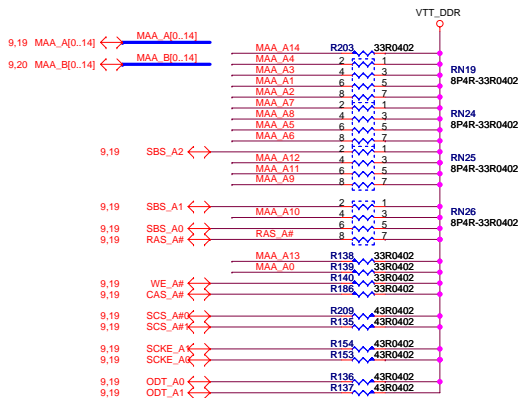
Tuesday, September 11, 2007

Sheet

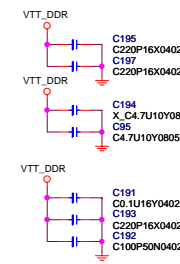
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of

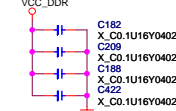
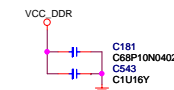
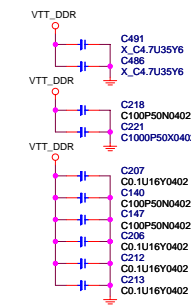
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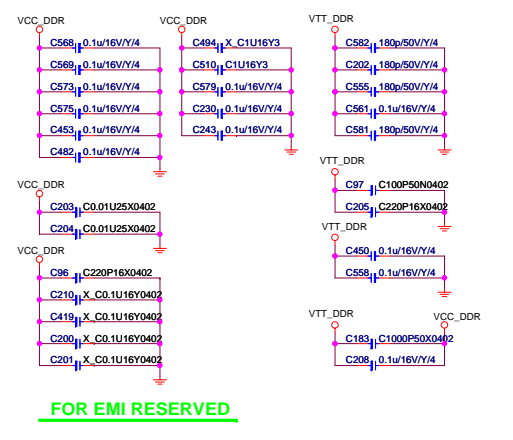
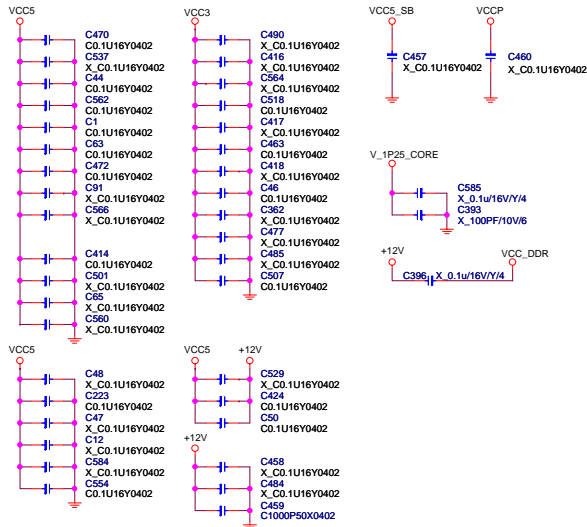
CHANNEL A V_SM_VTT DECOUPLING CAPS



CHANNEL B V_SM_VTT DECOUPLING CAPS

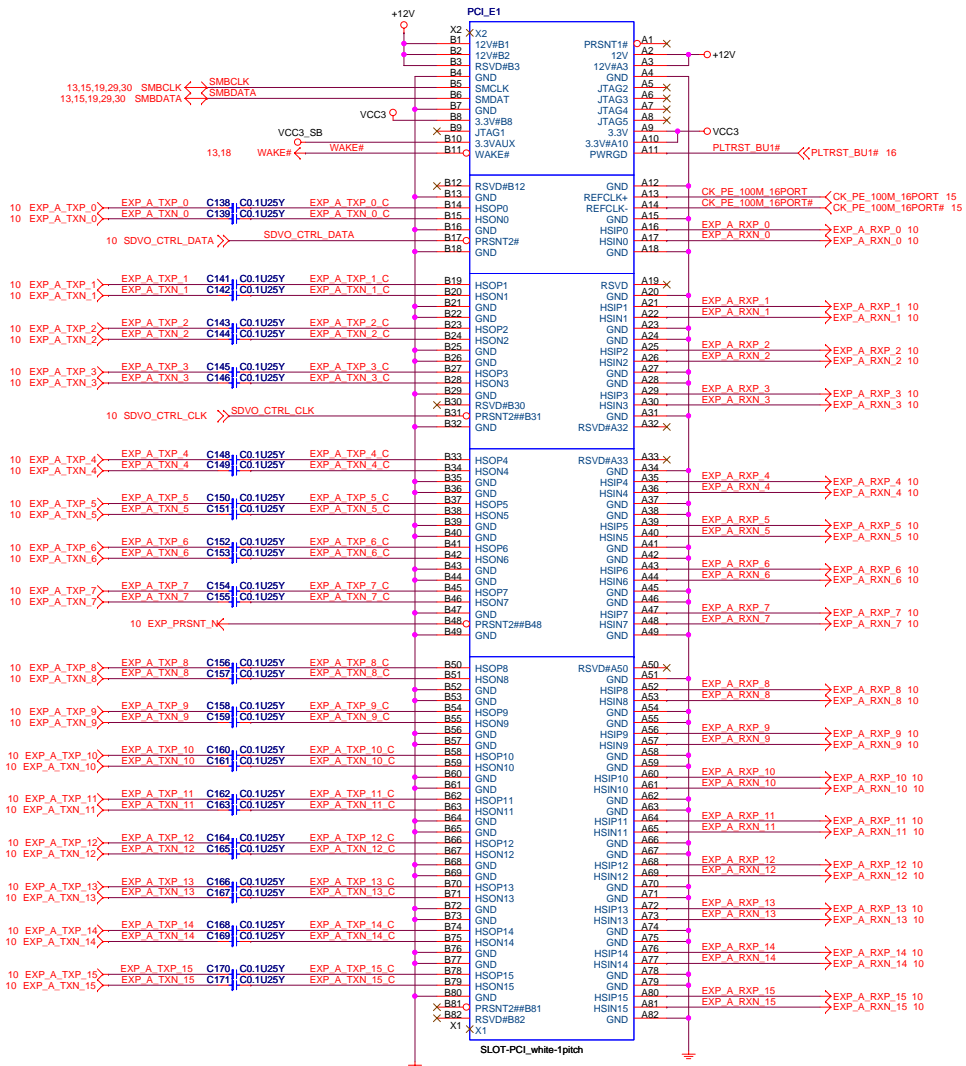


FOR EMI RESERVED

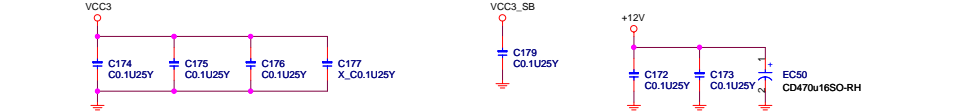
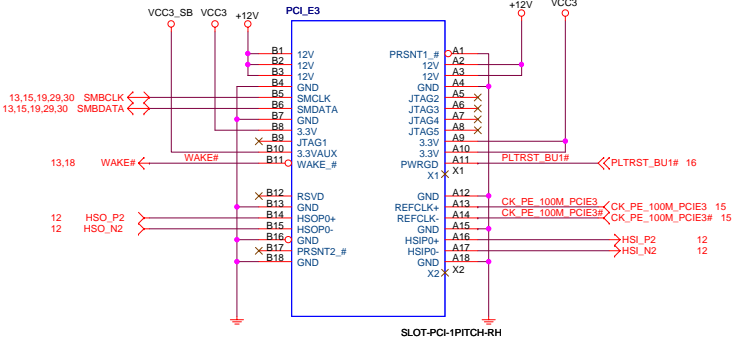
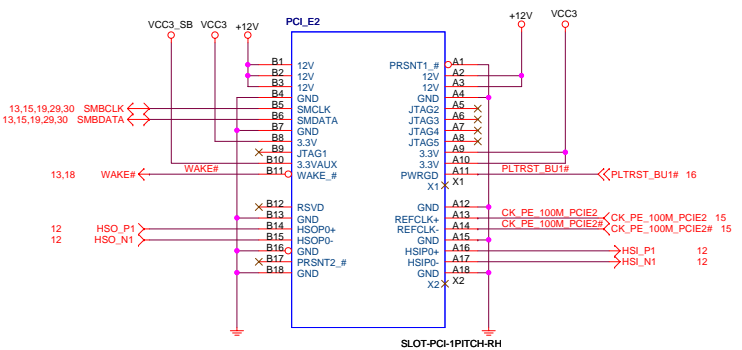


FOR EMI RESERVED

MICRO-STAR INT'L CO., LTD.		
Title		
DDR II VTT DECOUPLING		
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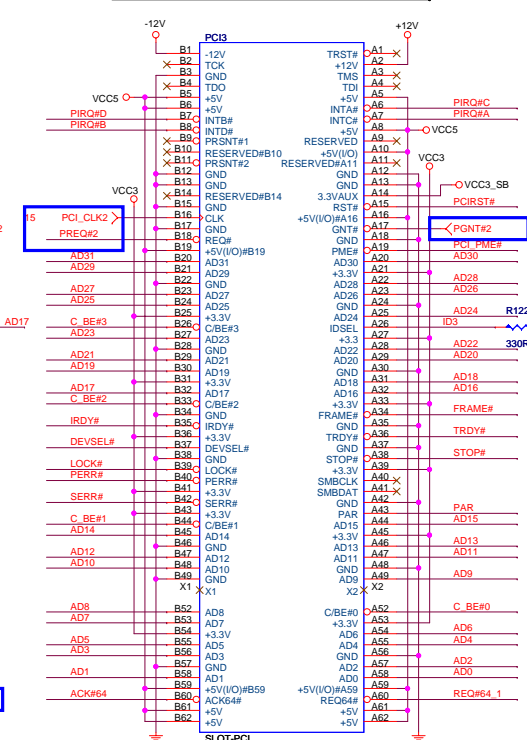


PCI EXPRESS 1-PORT

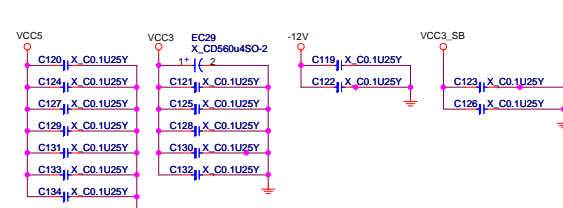


MICRO-STAR INT'L CO., LTD.		
Title PCI EXPRESS 16 & 1 PORT		
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PCI SLOT 3 (PCI VER: 2.2 COMPLY)

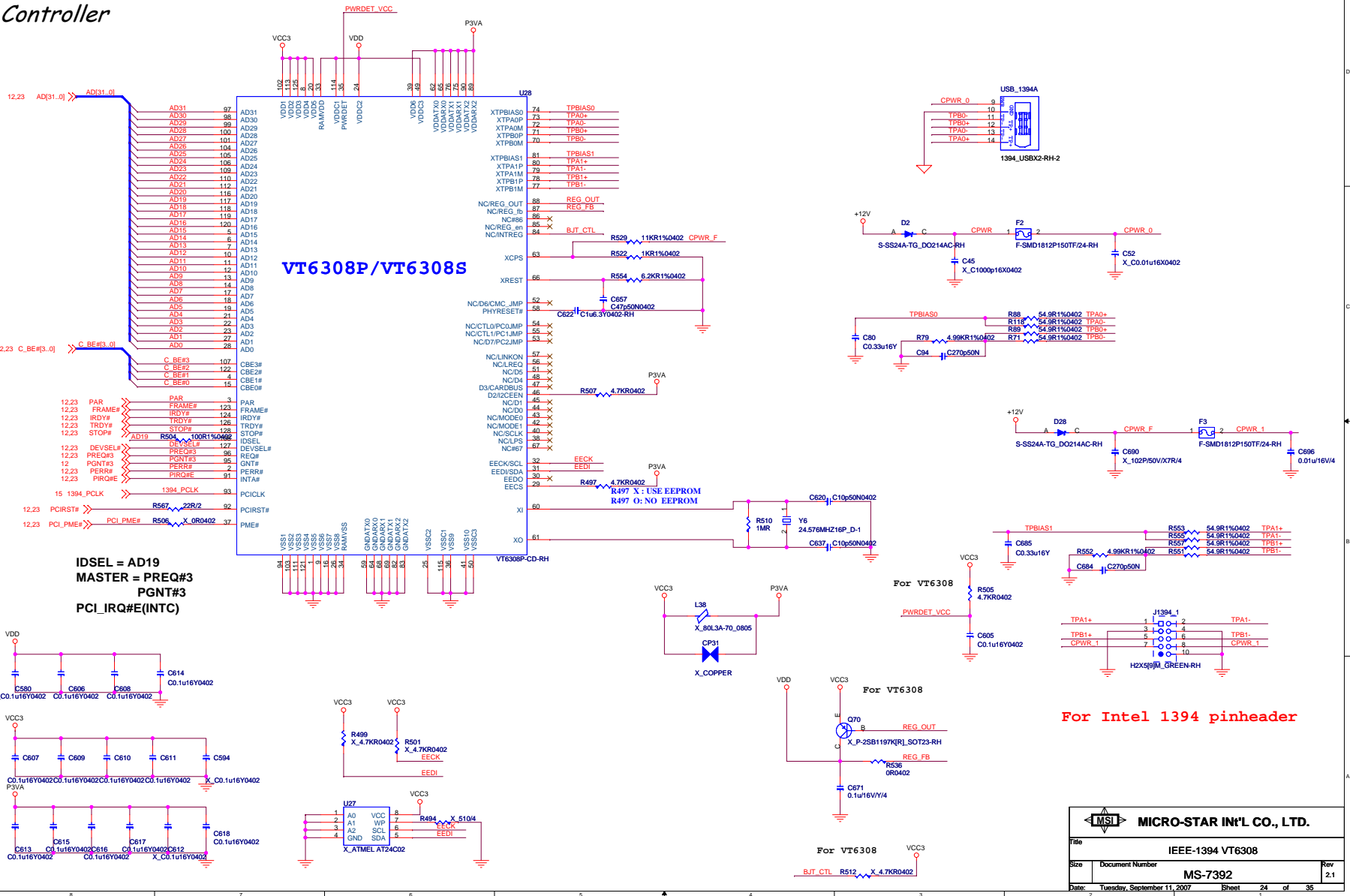


```
IDSEL = AD18
MASTER = PREQ#2
PIRQ#C
```



Title			
PCI 1~ 4 Slots			
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1394a OHCI Link Layer
Controller



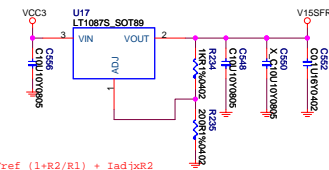
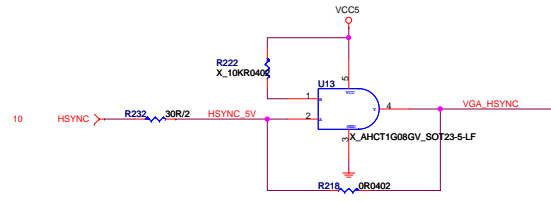
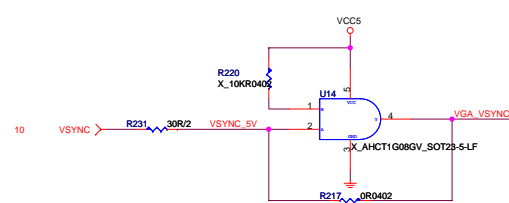
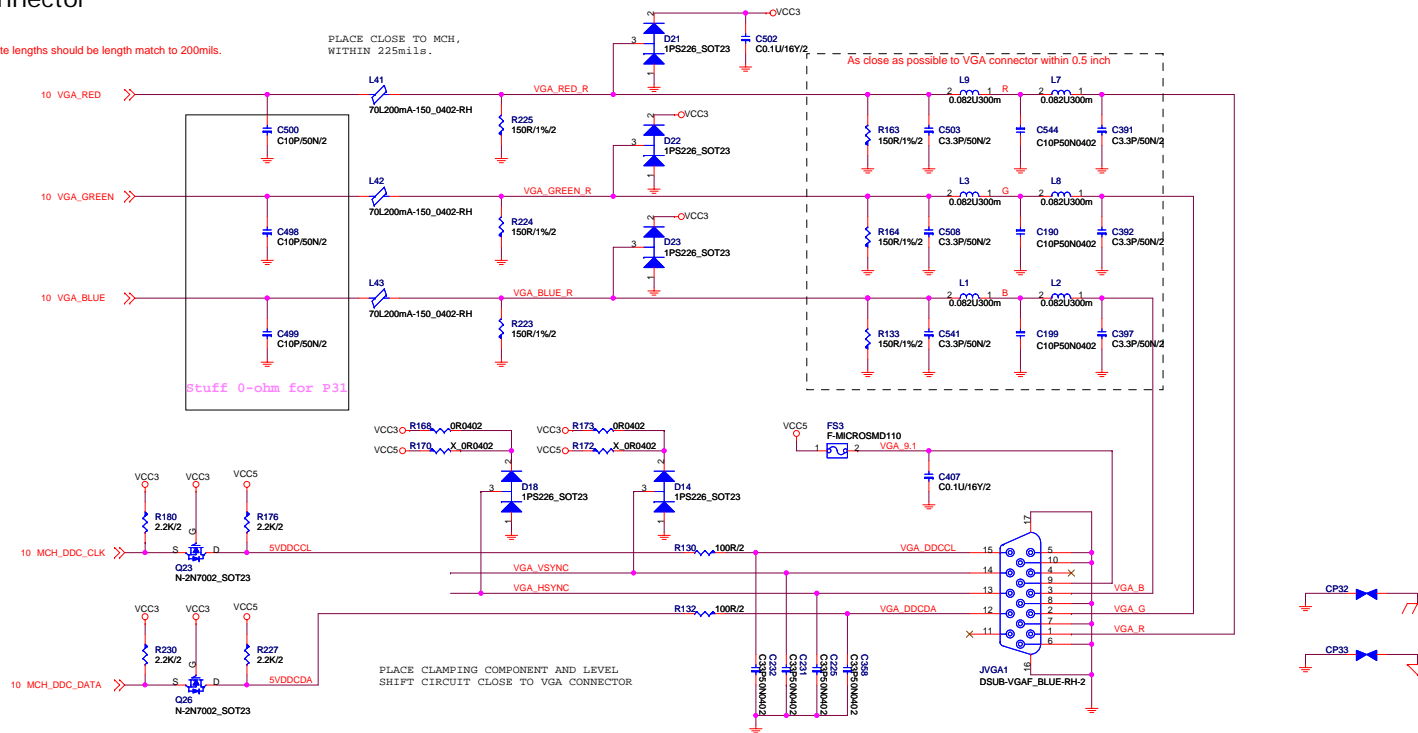
Video Connector

Thw R ,G ,B route lengths should be length match to 200mils.

PLACE CLOSE TO MCH,
WITHIN 225mils.

PLACE CLOSE TO VGA CONNECTOR

As close as possible to VGA connector within 0.5 inch



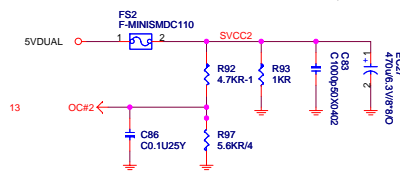
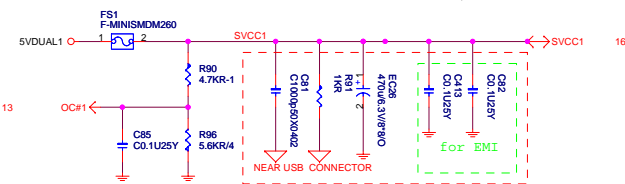
$V_o = V_{ref} (1 + R_2/R_1) + I_{adj} R_1$
where $V_{ref} = 1.25V$, $I_{adj} = 55\mu A$



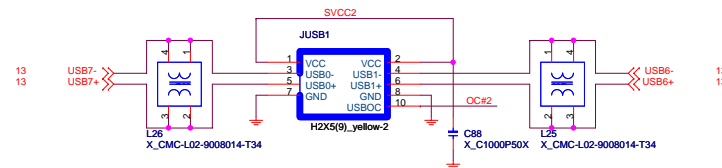
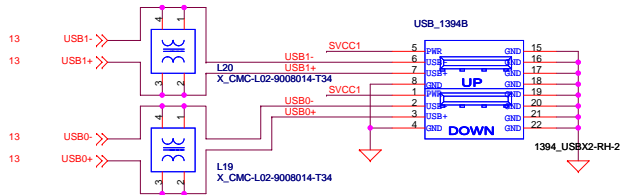
MICRO-STAR INT'L CO., LTD.

Title					ATA33/66/100 IDE & SATA Connectors					
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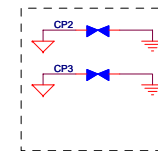
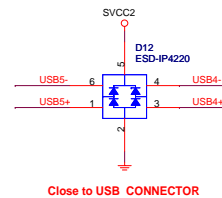
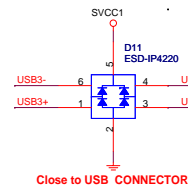
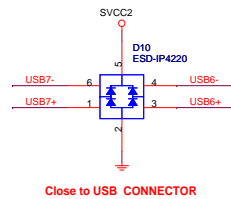
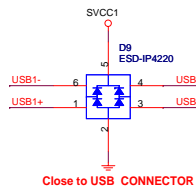
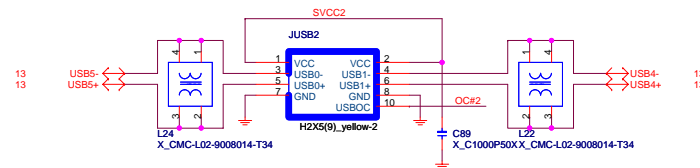
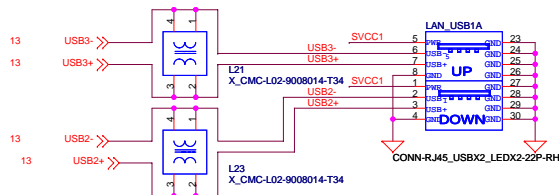
POWER CIRCUIT FOR USB PORT (FRONT)



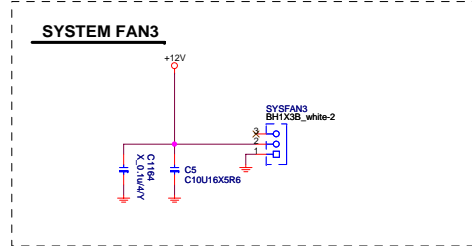
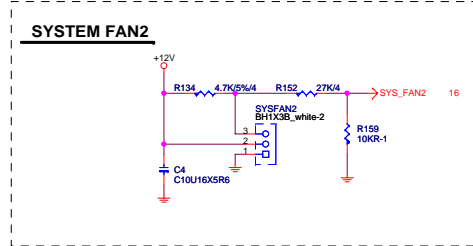
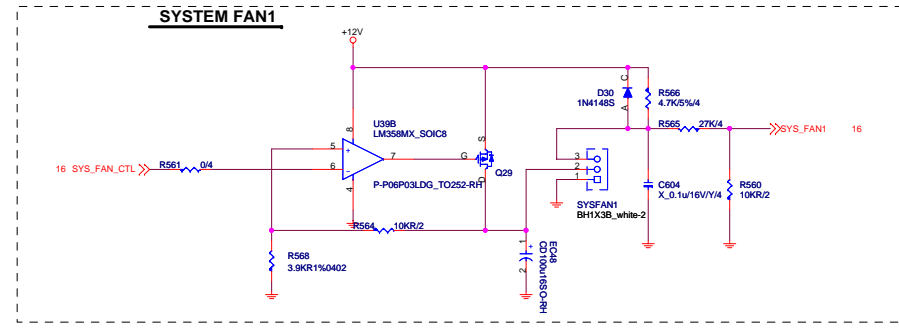
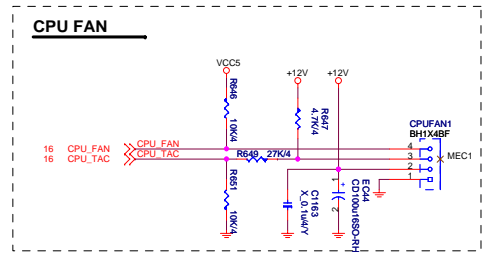
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



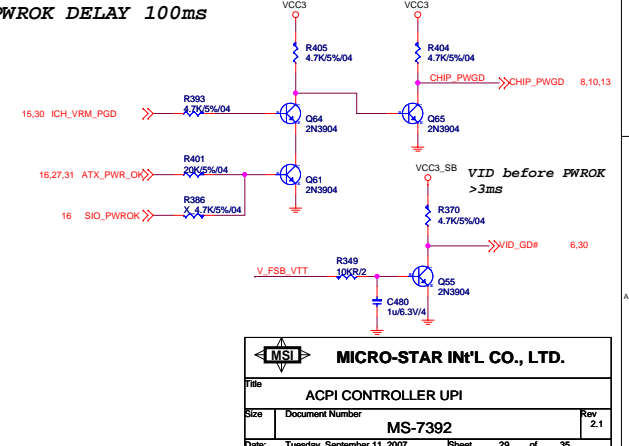
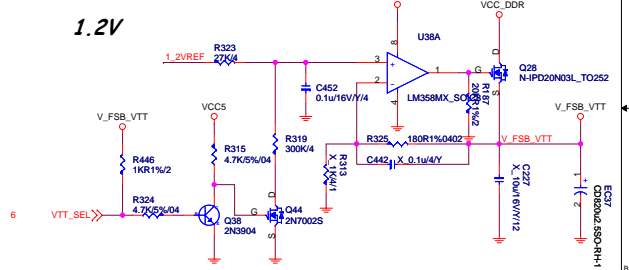
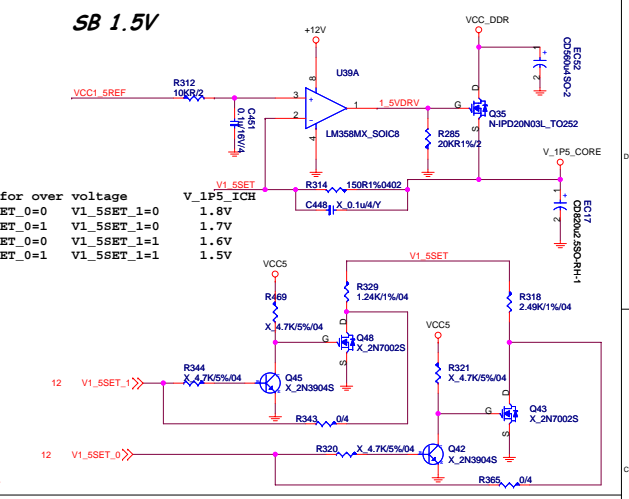
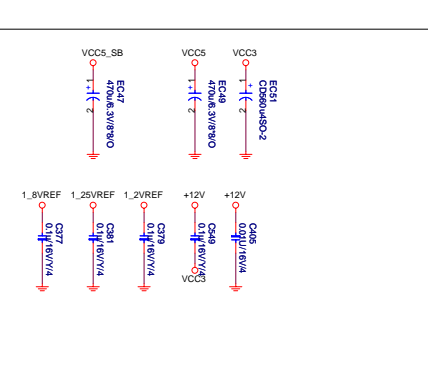
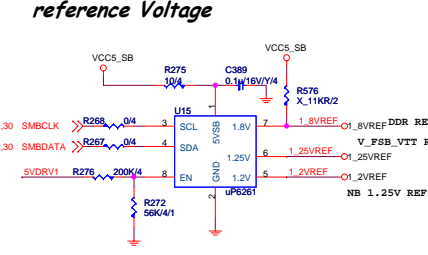
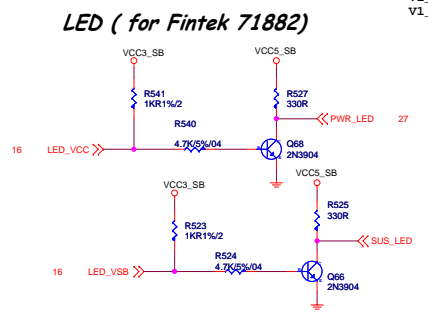
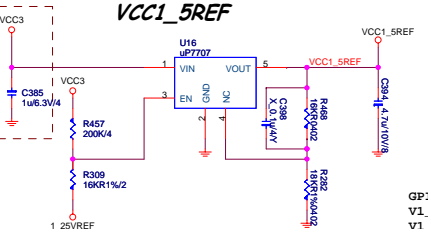
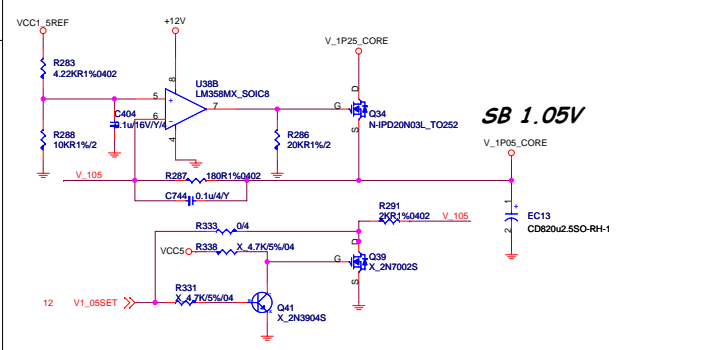
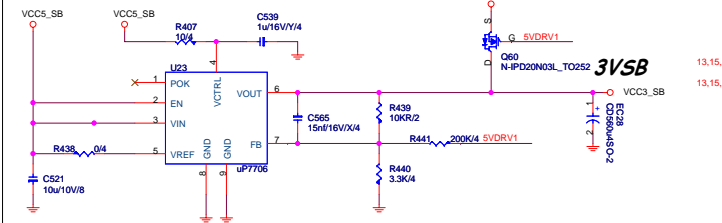
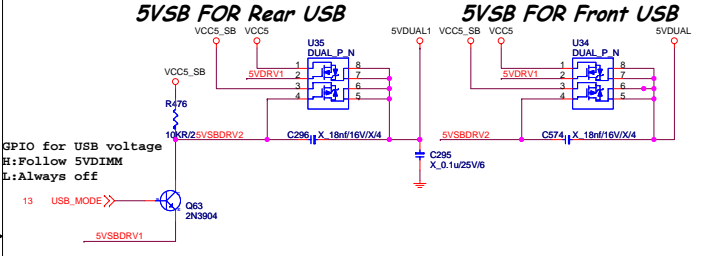
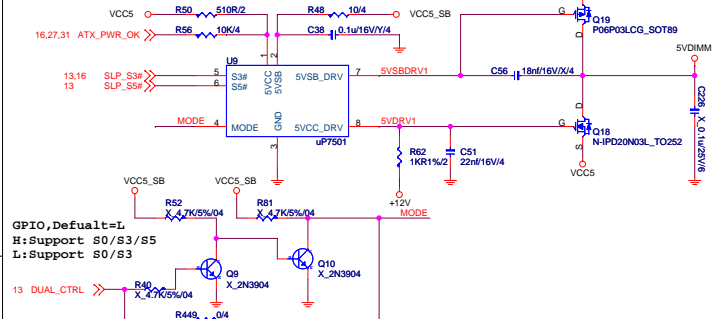
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



Title			
USB Connectors			
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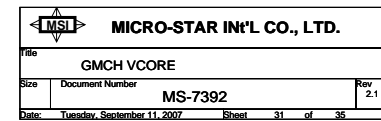
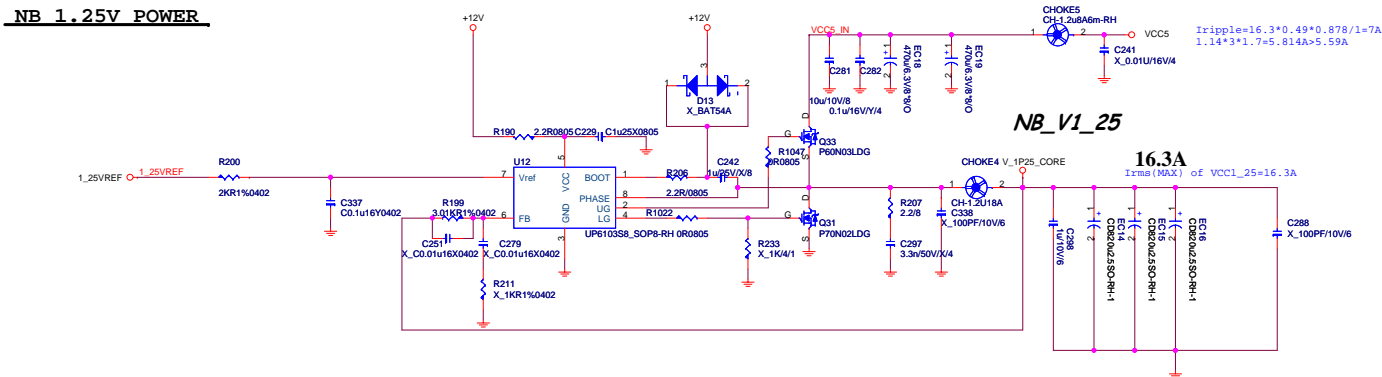


5VDIMM FOR
DDR



MSI MICRO-STAR INT'L CO., LTD.		
Title	ACPI CONTROLLER UPI	
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NB 1.25V POWER



Auto-BOM Manual Parts

PCB1
PCB
PCB-7392

BATTERY1
BATTERY-CR2032

Auto-BOM Option Parts

RTL8111B
OPT
X_RTL8111B

ICH7R
OPT
X_ICH7R

G31
OPT
X_G31

P31-R1
OPT
X_OR0402

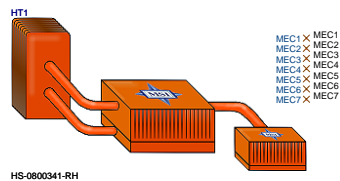
OnVGA1.3
OPT
X_1.3KR1%/2

G31-C1
OPT
X_C0.1U16V0402

P31 HEATSINK ICH7 HEATSINK

P31 HEATSINK
OPT
P31 HEATSINK

ICH7 HEATSINK
OPT
ICH7 HEATSINK



MEC1 X MEC1
MEC2 X MEC2
MEC3 X MEC3
MEC4 X MEC4
MEC5 X MEC5
MEC6 X MEC6
MEC7 X MEC7



MICRO-STAR INT'L CO., LTD.

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2.0 Change 2.1list:

- 1. Power team change :
Remove EC1009、EC1012、R1050;R1037=56K1%; RT1001=4.7K; R1046=10R1%
R1017=1.1K1%; R1014=910R1%; C1031=680p; R1045=100R; C1014=33p。 (page 30)
- 2. Add CK_25M_0F Pullup to VCC3_SB.(Page 15)
- 3. Add a test point for ICH SUSCLK signal
- 4. Add IDE reset for lever shift
- 5. Change CHOCK to new footprint

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ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	PIRQ#E
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	PIRQ#F
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	PIRQ#G
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	PIRQ#H
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	JAUD2_EN#
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	SMB_ALERT#
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	0	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	N/A	PGNT#5
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	1	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	1	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	PREQ#4
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC (NO CHANGE)
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	1	NC
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	0	NC
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	0	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	0	NC
GPIO29	DC5#	C3	I/O	Resume	N	N	3.3V	GPI	OC#2
GPIO30	DC6#	A2	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	OC#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	1	BIOS_WP#
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	1	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	0	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	1	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	PGNT#4
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39;36;23;21;19;7;0]; default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31;29;15;8]; default as inputs and should be pulled up to VccSus3_3 if unused.

SIO W83627EHF(CONTINUE)					
GPIO	Alt Func	PIN	USAGE	Input/Output	NOTES
GP44	DTRB#	81	DTRB#	OUT8	UART B Data Terminal Ready.
GP45	RTSB#	80	RTSB#	OUT8	UART B Request To Send.
GP46	DSRB#	79	DSRB#	INt	Data Set Ready.
GP47	CTSB#	78	CTSB#	INt	Clear To Send.
GP50	EN_VRM10/WDTO#	77	STRAPPED DOWN	INcd	defined as VID transition voltage level
GP51	RSMRST#	75	RSMRST#	OD12	Resume reset signal output.
GP52	SUSB#	73	SLP_S3#	INt	System S3 states input.
GP53	PSON#	72	PSON#	OD12	This pin generates the PWRCTL# signal while the power failure.
GP56	PSIN	68	PSIN	INtd	Panel Switch Input.
GP57	PSOUT#	67	PSOUT#	OD12	Panel Switch Output.
GP60	RIA#	57	RIA#	INt	Ring Indicator.
GP61	DCDA#	56	DCDA#	INt	Data Carrier Detect.
GP62	SOUTA/PENKBC	54	SOUTA	OUT8	UART A Serial Output.
GP63	SINA	53	SINA	INt	Serial Input.
GP64	DTRA#PENROM	52	DTRA#	OUT8	UART A Data Terminal Ready.
GP65	RTSA#HEFRAS	51	RTSA#	OUT8	UART A Request To Send.
GP66	DSRA#	50	DSRA#	INt	Data Set Ready.
GP67	CTSA#	49	CTSA#	INt	Clear To Send.

GPIO	PIN	POWER	TOL	SIGNAL NAME
FGPIO0	6	MAIN	3.3V	ATADET0
FGPI1	5	MAIN	3.3V	PULL UP
FGPI2	4	MAIN	3.3V	PULL UP
FGPI3	3	MAIN	3.3V	PULL UP
FGPI4	30	MAIN	3.3V	PULL DOWN

Note: FWH GPs should only be used for static options, do not put dynamic nets on these

PCI Config.				
DEVICE	MCPI INT	REQ#/GNT#	IDSEL	CLOCK
LAN	PIRQ#E	PREQ#4 PGNT#4	AD20	PCI_LAN
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1
PCI3	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD18	PCI_CLK2
PCI4	PIRQ#D PIRQ#A PIRQ#B PIRQ#C	PREQ#3 PGNT#3 PREQ#5 PGNT#5	AD19 AD21	PCI_CLK3 PCI_CLK4

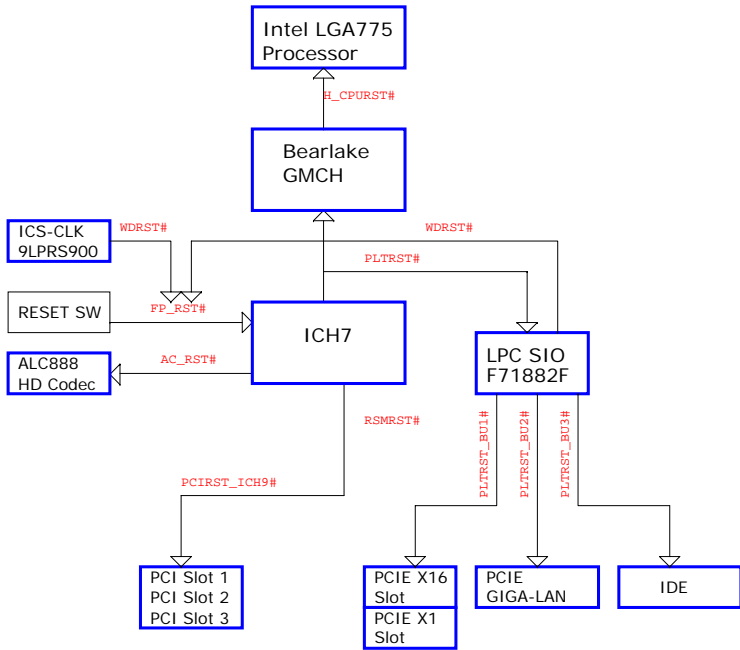
DDRII DIMM Config.		
DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM 2	A2H	P_DDR3_A/N_DDR3_A P_DDR4_A/N_DDR4_A P_DDR5_A/N_DDR5_A
DIMM 3	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B
DIMM 4	A6H	P_DDR3_B/N_DDR3_B P_DDR4_B/N_DDR4_B P_DDR5_B/N_DDR5_B

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

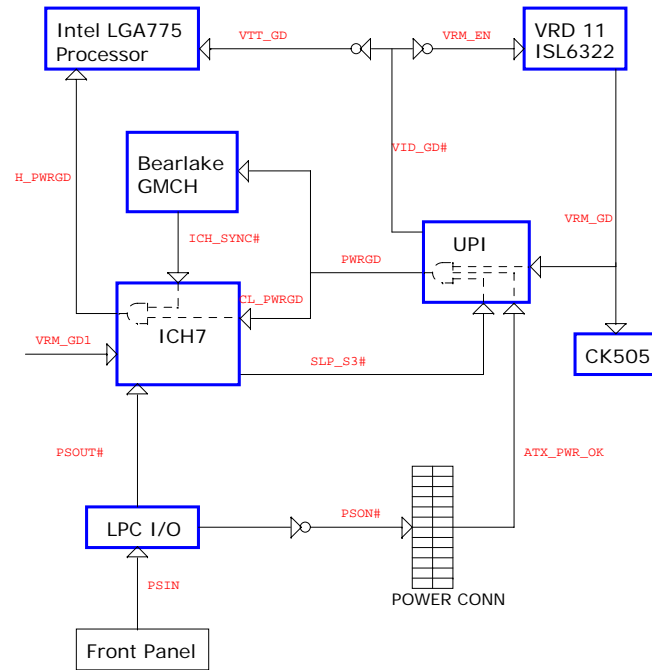
JCI1	Chassis Intrusion
Open	Normal
(1-2)	Chassis Open

GPIO MAP & JUMPER SETTING			
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RESET MAP



PWROK MAP



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